IN THE CLAIMS:

1. (Currently Amended) A network switch having an internet port interface controller, said internet port interface controller comprising:

a memory; and

a high performance interface for communicating with other switches and components through the transfer of data packets contained in said memory;

wherein said high performance interface comprises a data connection bus, where data is transferred on both a rising edge and a falling edge of a clock signal, the data connection bus has output drivers and a multiplexing circuit connected to the output drivers;

wherein said multiplexing circuit has two levels of glitchless multiplexors, with at least one output of an initial, first level of glitchless multiplexors is input into a second level of glitchless multiplexors containing at least one glitchless multiplexor, to serialize said data transmitted over said high performance interface.

2. (Currently Amended) A network switch as recited in claim 1, wherein said first level of glitchless multiplexors comprises two glitchless multiplexors, each having a first input, a second input, an output and control, and said second level of glitchless multiplexors comprises a single glitchless multiplexor, having two input points, an output point and a control point;

wherein said first level of glitchless multiplexors receives data from said data packets contained in said memory and the output of each of said two glitchless

multiplexors is connected to one of the two input points of said single glitchless multiplexor.

3. (Original) A network switch as recited in claim 2, wherein said multiplexing circuit further comprises two additional multiplexors, each having two input connections, an output connection and a control connection, wherein said data received from said data packets in input into said input connections of said additional multiplexors and said output connection of each of said additional multiplexors is connected to the first and second inputs of said first level of glitchless multiplexors.

4. (Original) A network switch as recited in claim 3, wherein the multiplexing circuit additionally comprises a plurality of flip flop circuits, each having an input port, and output port and clock input connected to said clock signal, to control the flow of data to said first level of glitchless multiplexors and said additional multiplexors.

5. (Original) A method of sending data through a high performance interface of a network switch, said method comprising the steps of:

receiving parallel data to be sent over said high performance interface;

multiplexing said parallel data;

storing a portion of said parallel data in a first register clocked on a positive edge of a clock signal;

storing another portion of said parallel data in a second register clocked on a negative edge of said clock signal;

inputting said portion into a first, first level glitchless multiplexor;

inputting said another portion into a second, first level glitchless multiplexor;

multiplexing said portion and said another portion, using said first level glitchless multiplexors, based on a multiplexor selection signal input into said first level glitchless multiplexors, and outputting the outputs of said first level glitchless multiplexors to a second level glitchless multiplexor;

multiplexing said data by selecting alternating inputs to be multiplexed onto outputs of said second level glitchless multiplexor, based on said multiplexor selection signal input into said second level glitchless multiplexor;

wherein each of said first level glitchless multiplexors produces a function hazard when more than one input to said first level glitchless multiplexor changes simultaneously;

wherein said step of multiplexing said data by selecting alternating inputs is timed such that said second level glitchless multiplexor only selects input from one of said first level multiplexors that is not producing said function hazard.